# A New Model for the Dual-Gate GaAs MESFET

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*Abstract*—**The development of a novel GaAs dual-gate MESFET model suitable for the design and analysis of microwave circuits is described. The model, a quasi-two-dimensional physical model, is numerically efficient due to a unique formulation of the carrier transport equations. The model includes a comprehensive description of the geometric and material parameters accounting for recess structures, nonuniform doping profiles, current injection into the buffer layer, forward-biased gate conduction, and surface depletion. The accuracy of the model under dc, small-signal, and large-signal operating conditions is assessed by comparing simulated and measured performance.**

## I. Introduction

THE DUAL-GATE FET (DGFET) has proved to be an extremely versatile device, as demonstrated by the wide variety of microwave applications for which the device has been considered. These have included mixers, amplifiers, phase shifters, switches, frequency multipliers, and frequency discriminators. Despite this, there is little evidence to suggest that the device is being widely incorporated into commercial circuits. The failure of the DGFET to find widespread use is due partly to the inability to analyze DGFET circuits accurately because of the absence of accurate and numerically efficient mathematical models for the device. Since the device generally operates under nonlinear conditions, it is essential that a model of the DGFET be capable of predicting this mode of operation if it is to be used for practical circuit analysis.

Previous attempts at describing the nonlinear behavior of the DGFET have concentrated on equivalent circuit models [1], [2], although analytical [3] and physical [4], [5] models have also been considered. Equivalent circuit models have not proved satisfactory for the modeling of DGFET's since several dc and RF measurements over a range of bias points are required to determine the circuit elements and their nonlinear behavior. Closed-form analytical models represent a compromise between equivalent circuit and physical models. These require empirical expressions, derived from either measured electrical performance or an understanding of the device physics, to characterize a given device. Physical simulations have the intrinsic capability to model all modes of device operation and require only the material and geometric details for the definition of the device. One-dimensional physical models, utilizing the gradual channel approximation, have been used to investigate the noise and gain performance of DGFET's [6], [7]. For modern devices, where the gate length to active layer thickness ratio exceeds the boundary conditions, more rigorous physical models need to be used.

This paper examines the application of physical modeling techniques to the characterization of the DGFET. A full two-dimensional model is described which, although capable of predicting device performance, is found to have only limited application due to its excessive computational requirements. However, the physical understanding obtained from the full two-dimensional model is used to develop a novel quasi-two-dimensional model for the device. The new model is shown to be numerically efficient and suitable for the accurate analysis of DGFET circuits.

## II. Physical Modeling of the DGFET

The full two-dimensional physical model uses the first two moments of the Boltzmann transport equation to describe the carrier transport processes. This formulation requires the solution of two equations. The first is the current continuity equation

$$\frac{\partial N}{\partial t} = \frac{1}{q}\nabla \cdot \boldsymbol{J} \tag{1}$$

where

$$\boldsymbol{J} = qN\mu\boldsymbol{E} + qD\nabla N \tag{2}$$

where $\boldsymbol{J}$ is the current density, $q$ the electronic charge, $\mu$ the electron mobility, $\boldsymbol{E}$ the electric field, $D$ the diffusion coefficient, and $N$ the electron density. The second equation is Poisson's equation:

$$-\nabla^2\psi = \frac{q}{\epsilon_0\epsilon_r}(N_d - N) \tag{3}$$

where $\psi$ is the potential, $N_d$ the doping concentration, and $\epsilon_0\epsilon_r$ the dielectric constant. Finite difference methods are used to solve these equations at each node of a regularly spaced rectangular mesh. With a mesh spacing of 0.02 $\mu$m in both dimensions and a mesh of $375 \times 31$ points, the model is suitable for modeling most commercially available devices.

Manuscript received November 30, 1988; revised April 18, 1989. This work was supported by Thorn Emi Electronics Ltd., Wells, England, and by the Science and Engineering Research Council.

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IEEE Log Number 8929887.

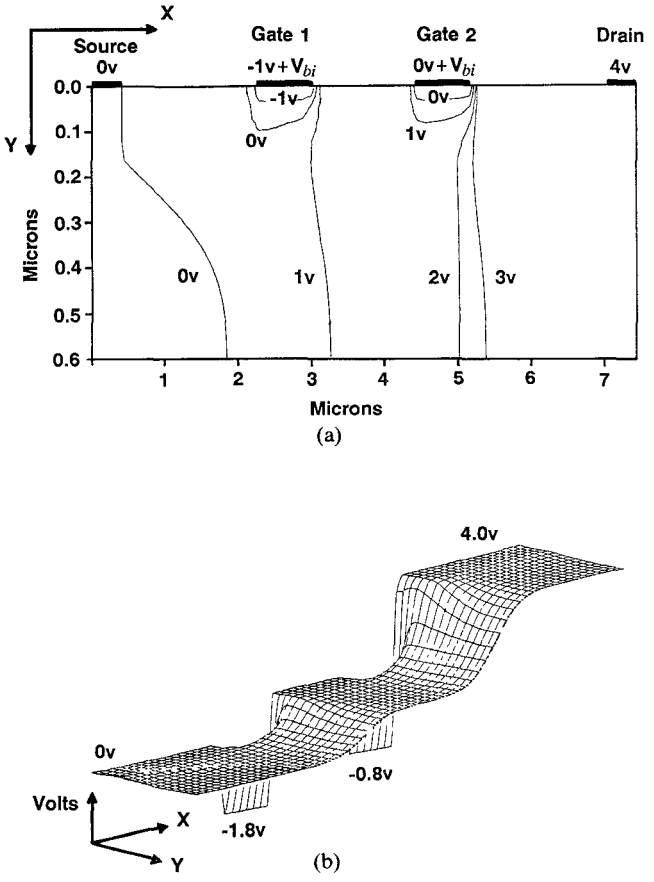


Fig. 1. (a) Contours of potential for a GaAs dual-gate FET ($V_{bi}$ is the built-in potential) and (b) three-dimensional representation of the potential distribution, obtained from the full two-dimensional simulation.

The simulation proceeds with the bias voltages applied to each contact but with the doping concentration throughout the device in an unperturbed state. The simulation time taken for the doping concentration to achieve a steady-state distribution consistent with the applied voltages defines the computer run time for the model. With a time step of 0.02 ps, this is typically 25 ps, which requires 2000 CPU seconds on an Amdahl 5860 mainframe computer. One of the advantages of the two-dimensional physical model is the insight that it gives into the operation of the device. This can clearly be seen in the two-dimensional contour plot and the three-dimensional representation of the potential distribution shown in Fig. 1(a) and (b) respectively. These results are for the simulation of a DGFET with geometric and material parameters as shown in Fig. 2. The potential distribution shows that, despite the negative bias applied to gate 1, the voltage drop across gate 2 is greater; that is, the effective negative bias on gate 2 is greater due to self-biasing.

The suitability of the model for analyzing RF performance has been investigated [5]. It was found that, for the simulation of a microwave mixer with an intermediate frequency (IF) of 5 GHz, over 7000 CPU seconds were required to simulate the first two cycles of the IF. Thus, although the model provides information on the nature of device behavior which could not be obtained from alternative models, the full two-dimensional model is impractical with regard to the analysis of DGFET microwave circuits.

The insight gained from the simulation into device operation has facilitated the development of a new physical model for the DGFET. The potential contours shown in Fig. 1(a) indicate that while the conducting channel is two-dimensional, the electric field within it can be assumed to be one-dimensional since the contours are virtually parallel. This assumption provides the basis for the development of a quasi-two-dimensional model in which the carrier transport equations are solved in one dimension and the two-dimensional aspects of device behavior are retained through the conducting channel description.

It has been observed from the simulation of submicron-gate-length MESFET's using a full two-dimensional energy-transport model that hot-electron effects play a significant role in the carrier transport processes [8]. For a 1.0-$\mu$m-gate-length single-gate FET it was shown that 10 percent of the device current was due to hot-electron effects; this increased to 30 percent for a 0.3-$\mu$m-gate-length FET. It is therefore essential that these effects be included in the device description if the model is to be applied to submicron-gate-length DGFET's. This has been achieved by using the hydrodynamic formulation of the semiconductor equations, which requires the solution of the Poisson, current continuity, energy conservation, and momentum conservation equations. Following the method of Cook and Frey [9], the energy conservation equation in one dimension is

$$\frac{\partial w}{\partial x} = \frac{3}{5}\left[qE - \frac{w - w_0}{v\tau_w(w)}\right] \tag{4}$$

where $w$ is the average electron energy, $\tau_w$ is the energy relaxation time, and $v$ is the electron velocity. The momentum conservation equation in one dimension is

$$v = \mu(w)\left[E - \frac{2\partial w}{3\partial x} - \frac{2w\partial N}{3N\partial x}\right]. \tag{5}$$

It is the inclusion of the second term in (5) that accounts for the energy contribution to the electron velocity; this term has been neglected in previously published quasi-two-dimensional models [10], [11]. It has been observed that the diffusion current term, $2w\partial N/3N\partial x$, is only significant where there are rapid changes in the electron concentration [12], and since this only occurs around the edges of the Schottky barrier depletion regions, the diffusion current contribution to the carrier transport process can be neglected.

The numerical efficiency of the model results from the formulation of the carrier transport equations. Following the technique of Carnez *et al.* [10], the carrier transport equations are reduced to a single quadratic in velocity, although the coefficients are more complex due to the inclusion of the spatial derivative of energy in (5). The model equations are solved in one dimension using finite difference methods with a space step of the order of 0.01

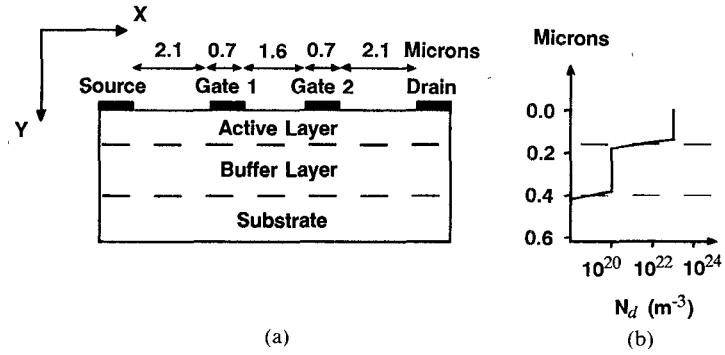


Fig. 2. (a) A cross section of the GaAs dual-gate FET modeled using the two-dimensional simulation and (b) doping profile.

$\mu$m. The boundary conditions for the simulation are the gate voltages and the source–drain current. A rigorous physical solution requires an iterative scheme to determine the physical parameters for a consistent solution to the carrier transport equations at each space step. This is necessary because the transport parameters $\mu(w)$ and $\tau_w(w)$ are determined from curve fits to Monte Carlo simulation results [10], [13] and cannot be updated until a new value of the average energy $w(x)$ has been obtained. Initial values for the parameters are defined from the value of the average energy at the previous step. However, it has been observed that there is little change in $\mu(w)$ and $\tau_w(w)$ between space steps, so the iterative scheme can be neglected without adversely degrading the accuracy. The displacement current term, $\epsilon_0\epsilon_r dE/dt$, which is included in the transport equations for RF simulations, requires an additional iterative scheme.

The conducting channel is defined by

$$Y_{\text{ch}}(x) = Y_a + Y_s\left[1 - \frac{N_d}{N(x)}\right] \tag{6}$$

with

$$Y_a = A(x) - Y(x) \tag{7}$$

where $Y_a$ is the undepleted active layer thickness, $A(x)$ is the active layer thickness, and $Y(x)$ is the depleted channel thickness. The empirical factor $Y_s$, the magnitude of which lies in the range 0.1 $\mu$m to 0.5 $\mu$m for typical MESFET structures [14], accounts for the penetration of the electrons into the buffer layer. For recessed gate structures $A(x)$ will be a function of $x$. $Y(x)$ is defined by either surface depletion or the Schottky barrier depletion regions with an abrupt transition assumed between the depleted and undepleted channel regions.

The Schottky barrier depletion region model used in this simulation is a hybrid of two previous models. The source side of each gate is modeled by using an elliptic approximation based on the analysis of the depletion region profiles published by Wasserstrom and McKenna [15]. The drain sides are modeled using a modified form of a model used by Sandborn *et al.* [11]. Ladbrooke *et al.* [16] have observed that the occupancy of the surface states is GaAs MESFET's is bias dependent and that the surface states have a pronounced effect on the microwave performance. This is taken into account by using a variable surface potential model, with the surface depletion thickness $Y_{sd}$ for the gate 1–source region defined by

$$Y_{sd}(x) = \frac{2\epsilon_0\epsilon_r}{qN_d}\left[\phi_{sd} + v_{\text{ch}}(x) - \frac{v_{gs1}}{L_{SG1}}\right] \tag{8}$$

where $\phi_{sd}$ is the built-in surface potential, $v_{\text{ch}}$ is the channel potential, $v_{gs1}$ is the gate 1–source potential, and $L_{SG1}$ is the source–gate separation. Similar expressions exist for the surface depletion thickness in the intergate region and the gate 2–drain region.

Nonuniform doping profiles have been included in the device description by following the technique of Shur and Eastman [17], which determines an effective doping density $N_d^-$ and channel thickness $\bar{A}$ from $A(y)$ and $N_d(y)$. The effective doping density and channel thickness thus obtained replace $N_d$ and $A$ is the model equations.

Forward conduction of the gate contacts is modeled using a thermionic-emission-diffusion model of the form

$$I_g = ZJ_0\exp\left(\frac{qV_B}{nkT}\right)\left[1 - \exp\left(-\frac{qV_B}{kT}\right)\right] \tag{9}$$

where

$$J_0 = A^{**}T^2\exp\left(-\frac{qV_{\text{bi}}}{kT}\right) \tag{10}$$

where $V_B = V_g - V_{\text{ch}}(x)$, the voltage drop across the barrier for x about the depletion regions, $k$ is Boltzmann's constant, $T$ is the temperature, $A^{**}$ is the effective Richardson constant ($1.44\times10^6$ $\text{m}^{-2}\text{K}^{-2}$), $Z$ is the gate width, $V_{\text{bi}}$ is the built-in potential of the Schottky barrier, and $n$ is the ideality factor. The accuracy of this model has been verified for GaAs Schottky barriers by Rhoderick [18]. Two schemes for calculating the gate currents have been considered. The conventional approach, where the current is determined from the gate–source voltage directly, has been compared with an iterative scheme. The iterative scheme is used to find the gate and source currents that are consistent with the voltage drop across the Schottky barrier depletion regions.

The specific contact resistivity, the metallization thickness, and the contact areas are used to determine the impedances associated with these fabrication-dependent

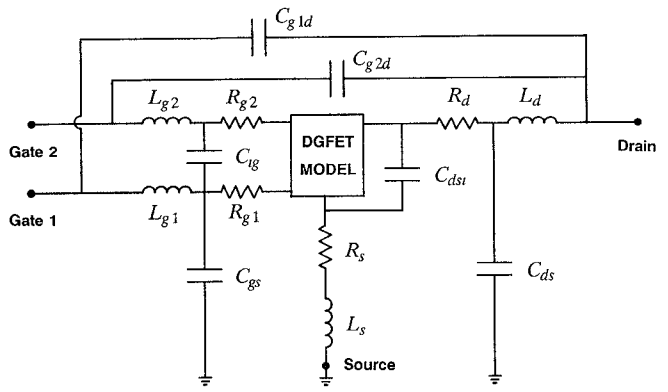


Fig. 3. The quasi-two-dimensional model and its parasitic circuit elements used for the simulation of the three-port $S$ parameters.

parameters. The nature of the gate metallization is required so that the built-in voltage can be specified.

## III. DC Simulation

The simulation has been implemented on an Amdahl 5860 mainframe computer. A single dc bias point requires less than 0.1 CPU second, which is more than 20000 times faster than the full two-dimensional simulation. The model may be used to determine the nonlinear behavior of the intrinsic elements of an equivalent circuit model for the DGFET under the quasi-static approximation. This would yield a numerically efficient large-signal model for the DGFET. However, in order to overcome the inherent limitations of the quasi-static approximation the model has been applied directly to the analysis of microwave circuits.

## IV. Small-Signal Simulation

The $S$ parameters for the DGFET are determined from the quasi-two-dimensional model in a simple three-step procedure. A combination of small-signal sinusoids are applied about a fixed dc bias operating point to enable the three port admittance, or $Y$, matrix to be calculated. Initially a signal is applied to gate 1 for an RF open circuit at the drain and an RF short circuit at gate 2. For the second step both gates are RF short-circuited with a small-signal drain current imposed. Finally, small-signal sinusoids are applied to both gates with the drain held at a short circuit to RF. For each step a set of time-varying gate currents and drain voltage are obtained. This provides enough information, with some redundancy, for the three-port $Y$ matrix to be determined. The redundant information is used to ensure that the overall procedure is consistent.

The $Y$ matrix thus calculated represents only the intrinsic device. It remains for the intrinsic parasitics (metallization resistances and intercontact capacitances) and the package parasitics (bond wire impedances and package capacitances), shown in Fig. 3, to be included in the device description. The elements are successively added to the device by adding the series elements to the $Z$ matrix and the parallel elements to the $Y$ matrix. The order in which the elements are added is shown in Table I. Finally the

TABLE I
The Order for Embedding the Parasitics to the Intrinsic Device Model

| Step | Elements Added | Matrix |
|---|---|---|
| 1 | $C_{dsi}$ | Y |
| 2 | $R_{g1}$, $R_{g2}$, $R_d$, $R_s$, $L_s$ | Z |
| 3 | $C_{ig}$, $C_{gs}$, $C_{ds}$ | Y |
| 4 | $L_{g1}$, $L_{g2}$, $L_d$ | Z |
| 5 | $C_{g1d}$, $C_{g2d}$ | Y |

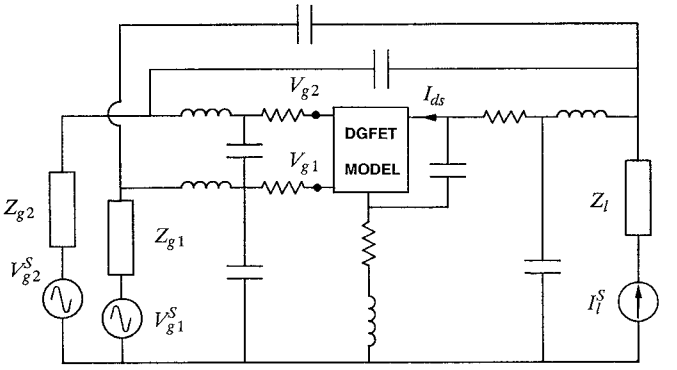


Fig. 4. The dual-gate FET circuit used for large-signal analysis.

$S$-parameter matrix for the embedded device is obtained. A set of three-port $S$ parameters from 2 to 18 GHz in 1.0 GHz steps takes 100 CPU seconds on a mainframe computer.

## V. Large-Signal Simulation

The application of the model to the analysis of mixer circuits required the development of an efficient large-signal algorithm. The algorithm employs the harmonic balance method [19], which partitions the circuit into linear, frequency-domain and nonlinear, time-domain parts. Large-signal equivalent circuit models often require two iteration schemes: a time-domain scheme to determine the dependent nonlinear device variables (voltages and/or currents) and a large-signal algorithm to determine the steady-state solution. This approach is unsuitable for circuits where the nonlinear device is described by a physical model because the computational effort required to achieve the steady state would be excessive. Thus, to improve the numerical efficiency a large-signal algorithm has been developed that avoids the need to iterate within the time domain. Consider the circuit of Fig. 4, which shows the physical model embedded in a linear circuit consisting of parasitic elements, the termination impedances at each port ($Z_{g1}$, $Z_{g2}$, and $Z_1$), and the applied voltages and current ($V_{g1}^S$, $V_{g2}^S$, and $I_1^S$). On applying Kirchhoff's laws to the circuit three coupled frequency-domain equations are

obtained:

$$L_A V_{g1} + L_B V_{g2} + L_C I_{ds} = f_1(V_{g1}, V_{g2}, I_{ds}) \quad (11)$$

$$L_D V_{g1} + L_E V_{g2} + L_F I_{ds} = f_2(V_{g1}, V_{g2}, I_{ds}) \quad (12)$$

$$L_G V_{g1} + L_H V_{g2} + L_I I_{ds} = f_3(V_{g1}, V_{g2}, I_{ds}) \quad (13)$$

where $L_A - L_I$ contain elements of the linear circuit, and $f_1$, $f_2$, and $f_3$ are nonlinear functions defined by the physical model.

The algorithm proceeds with estimates for the dc and applied RF signal components of the independent variables $V_{g1}$, $V_{g2}$, and $I_{ds}$. The gate currents and drain voltage are then determined from the physical model. Using a fast Fourier transform, the frequency-domain equivalents of these time-domain signals are obtained, the nonlinear functions are then calculated, and (11)–(13) are solved for $V_{g1}$, $V_{g2}$, and $I_{ds}$ for each frequency component. These new values of $V_{g1}$, $V_{g2}$, and $I_{ds}$, identified by the superscript $L$, will be different from the initial estimates; to reach the steady-state solution the differences between $V_{g1}$ and $V_{g1}^L$, $V_{g2}$ and $V_{g2}^L$, and $I_{ds}$ and $I_{ds}^L$ have to be minimized. This is achieved by updating the independent variables by using the method of Hicks and Kahn [20]. The estimate of $V_{g1}$ for the $k$th iteration is determined from

$$V_{kg1} = pV_{(k-1)g1} + (1-p)V_{(k-1)g1}^L \quad (14)$$

and similarly for $V_{kg2}$ and $I_{kds}$. The convergence parameter $p$ determines the rate of convergence and the stability of the large-signal algorithm. Although Hicks and Kahn proposed an iterative method for updating the convergence parameter to optimize the rate of convergence, a constant value of 0.9 for $p$ was found to give consistent behavior over a range of bias conditions and drive levels. The waveforms continue to be updated until a steady-state solution is reached. Convergence is said to be achieved when, for each harmonic component at each port, the voltage reflection coefficient between the linear and nonlinear networks is better than $-40$ dB. Typically 50 iterations are required for convergence to be attained; this requires 250 CPU seconds on a mainframe computer. For high drive levels and those cases where forward conduction through the gates becomes significant additional iterations are needed.

The number of frequency components considered in the circuit analysis is determined by the circuit application. Truncation of the spectral components is achieved, if required, by assuming that short-circuit terminations exist at both gates and that an open-circuit termination exists at the drain for spectral components beyond the highest frequency of interest.

## VI. Verification of the Model

To assess the behavior of the model under dc, small-signal, and large-signal operation, measurements were made on a commercial device. The Plessey P35-1310 device was selected since the geometric and material parameters for this device were available—with the exception of the active layer thickness, for which the manufacturing tolerances were specified. When these limits were included in the device description the range in the simulated $I_{dss}$ was 43 mA to 100 mA, shown in Fig. 5, which is in excellent agreement with variation in this parameter given in the manufacturer's data sheet [21]. Similar agreement was observed in the variation in the pinch-off voltage.

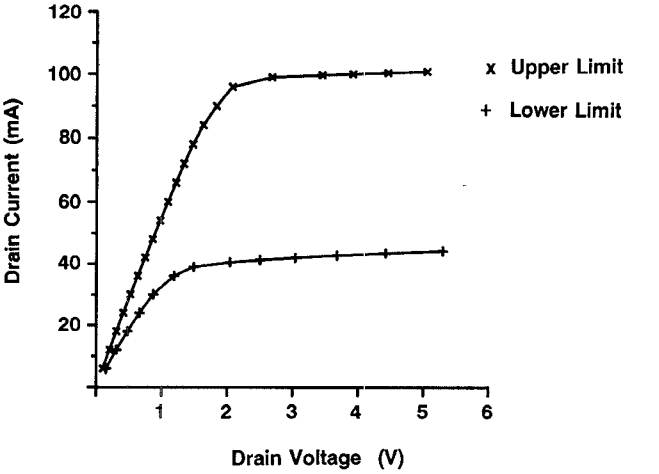


Fig. 5. The variation in the simulated $I_{dss}$ for the Plessey P35-1310 dual-gate GaAs FET is shown for upper and lower limits in active layer thickness ($V_{g1} = V_{g2} = 0$ V).

The transfer characteristics and quasi-static transconductance were measured using a HP 4145A semiconductor parameter analyzer. For a number of bias conditions the measured and simulated transfer characteristics are shown in Fig. 6. Measured and a simulated values of $g_{m2}$ are shown in Fig. 7. The active layer was varied to obtain the best fit between measured and simulated performance. The agreement is generally excellent for all of the transfer characteristics, which indicates that the interaction between the gate contacts is being correctly modeled. The discrepancies that occur for high drain currents, which coincide with regions of apparent negative output conductance in the measured data, are due to thermal heating effects. At present the model does not account for heat generation and flow although the transport parameters are a function of lattice temperature.

Forward gate conduction was also investigated experimentally. The gate 2 current versus drain voltage for $V_{g2} = 1.0 =$ V, $V_{g1} = 0$ V is shown in Fig. 8. Note that there is a "background current" of $1 \times 10^{-7}$ A due to surface leakage current, a phenomenon not included in the device description. The measured data were used to determine the ideality factor $n$, which was found to be 1.52 for gate 2. It is interesting to note that $n$ for gate 1 was found to be 1.47; the difference in $n$ between the two gate contacts is indicative of fabrication process variations. Also shown in Fig. 8 are results obtained by using both iterative and direct methods for calculating gate current within the simulation. The results for the noniterative technique were obtained by defining $V_B$ as the voltage drop between the gate contact and the beginning of the depletion region.

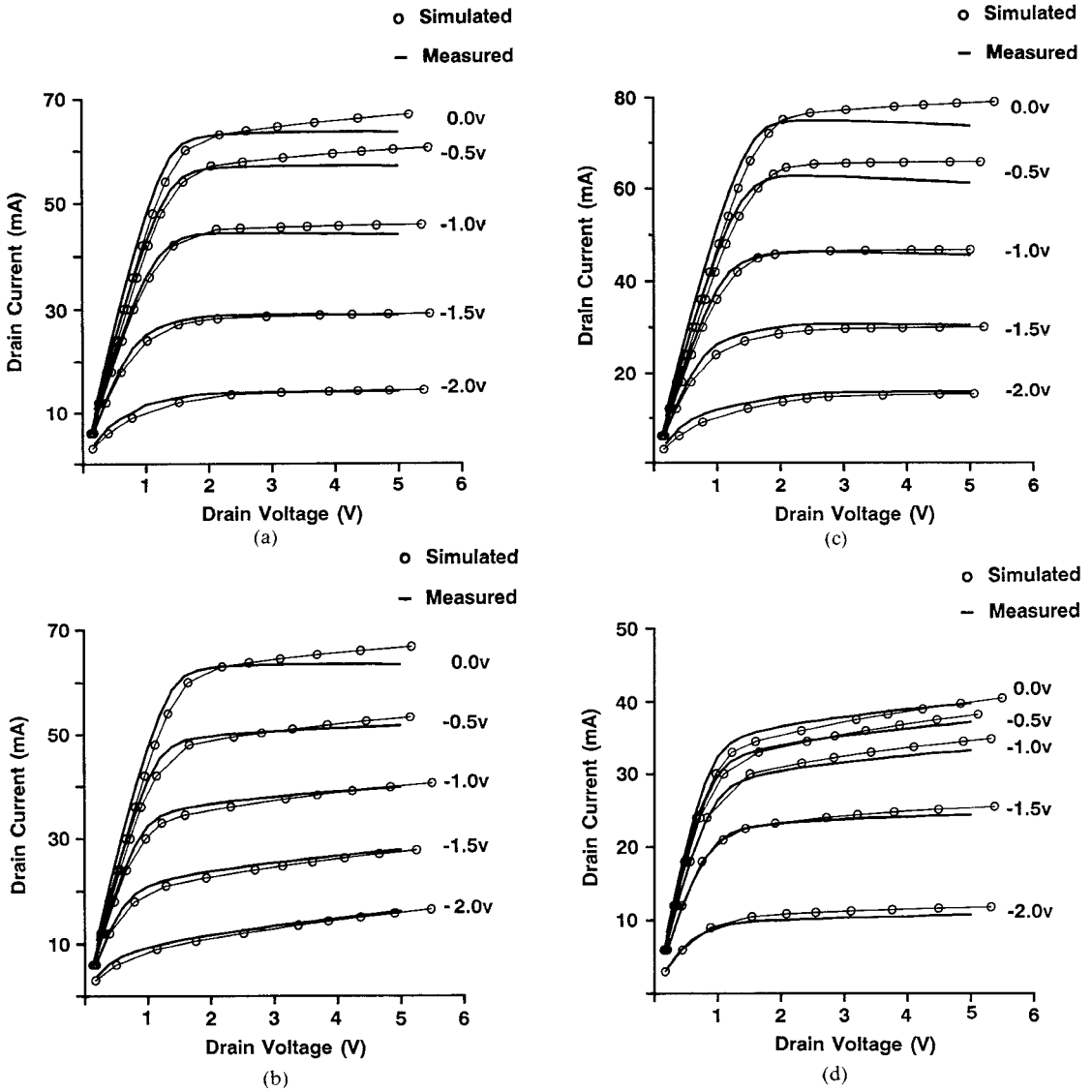


Fig. 6. Comparison of measured and simulated transfer characteristics for the Plessey P35-1310 dual-gate GaAs FET: (a) $V_{g1}$ varying, $V_{g2} = 0.0$ V; (b) $V_{g2}$ varying, $V_{g1} = 0.0$ V; (c) $V_{g1}$ varying, $V_{g2} = 0.5$ V; (d) $V_{g1}$ varying, $V_{g2} = -1.0$ V.

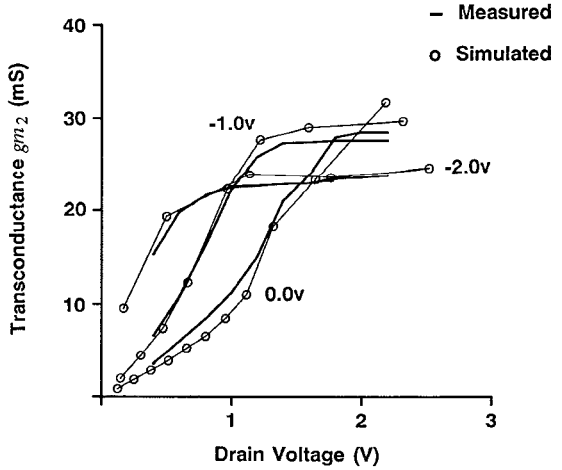


Fig. 7. Comparison of measured and simulated quasi-static transconductance for the Plessey P35-1310 dual-gate GaAs FET ($V_{g2}$ varying, $V_{g1} = 0.0$ V).

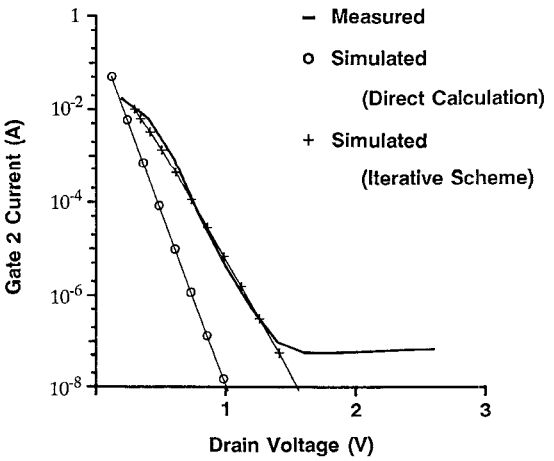


Fig. 8. Comparison of measured and simulated forward biased gate conduction for the Plessey P35-1310 dual-gate GaAs FET ($V_{g1} = 0.0$ V, $V_{g2} = 1.0$ V).

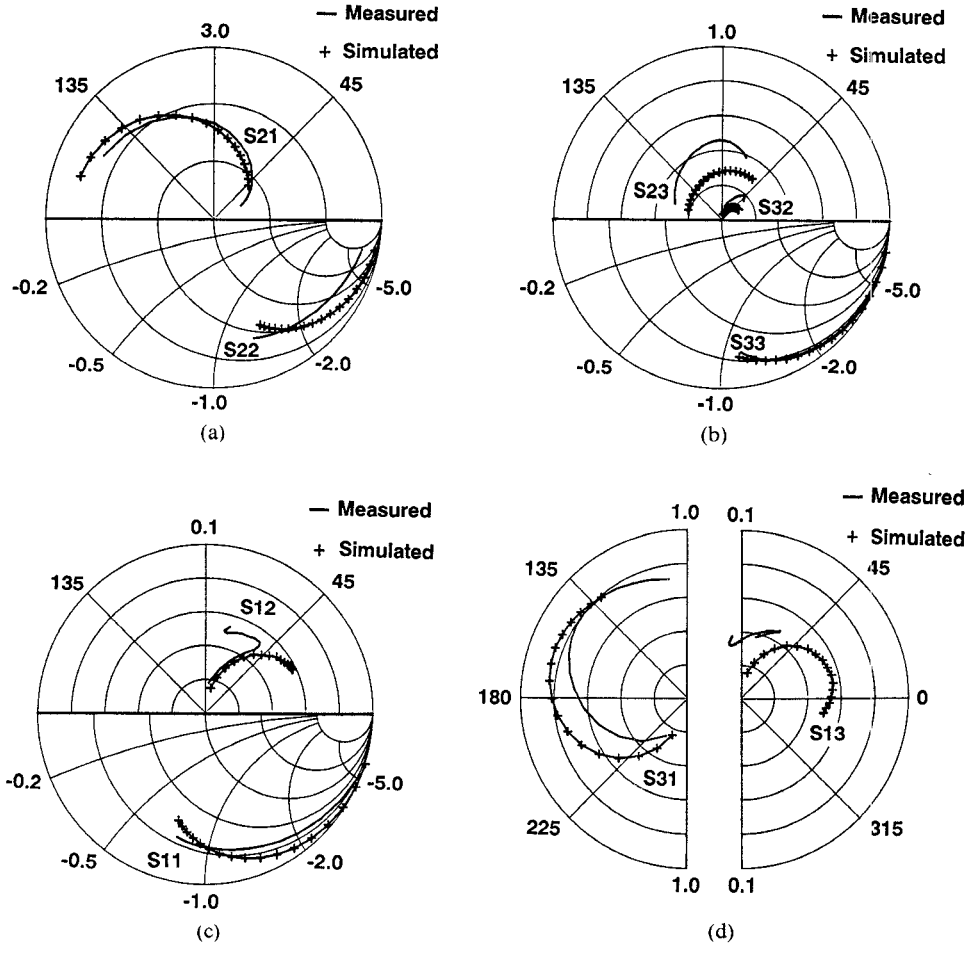


Fig. 9. Comparison of measured and simulated three-port $S$ parameters for the Plessey P35-1310 dual-gate GaAs FET: (a) $S22$, $S21$; (b) $S23$, $S32$, $S33$; (c) $S11$, $S12$; (d) $S31$, $S13$.

The superior accuracy of the iterative technique is clearly visible.

The development of an efficient optimization routine [22] enabled the parasitic elements shown in Fig. 3 to be de-embedded from the data sheet $S$ parameters. It was necessary to optimize only the parasitic elements since the intrinsic circuit elements were defined by the physical model. The simulated and measured $S$ parameters are shown in Fig. 9. While the agreement is not exact for each of the nine $S$ parameters, the correct trends are evident. The discrepancies are due in part to anomalies in the measured data and the relatively simple lumped element circuit used to describe the parasitics.

To evaluate the behavior of the model under nonlinear conditions the performance of a simple mixer circuit was investigated. The circuit was fabricated in suspended substrate stripline and consisted of a transmission line with a nominal characteristic impedance of 50 Ω terminated to RF in 50 Ω at each port. This simple circuit topology was selected to simplify the modeling of the microwave circuit, which enables the emphasis to be placed on the comparison between the measured and the simulated nonlinear behavior of the DGFET. The measured and the simulated variation in power output of the significant frequency components with local oscillator power are shown in Fig.

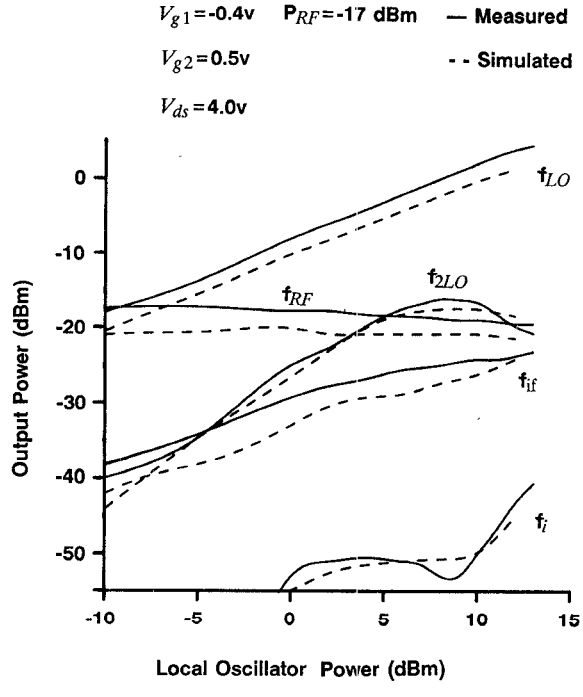


Fig. 10. Comparison of measured and simulated output power variation for the local oscillator and its second harmonic ($f_{LO}$, $f_{2LO}$), the intermediate ($f_{if}$), the RF ($f_{RF}$), and the image ($f_i$) frequency components with local oscillator power.

10 for a mixer with a local oscillator of 10 GHz and an RF signal of 11 GHz and power of −17 dBm. The overall agreement between measured and simulated performance is good although there are differences of up to 4 dB between some of the components. The discrepancies are principally due to the description of the parasitics used in the model.

## VII. Conclusions

A new, comprehensive model for the DGFET has been described. The combination of a numerically efficient physical model and a harmonic balance large-signal algorithm provides a powerful tool for the investigation of DGFET nonlinear circuit behavior. Since the device description is defined by the fundamental processing parameters, the sensitivity of device and circuit performance to processing variations can be investigated. Note also that the complex measurement procedures required for the definition of equivalent circuit models of the DGFET are to a large extent avoided since the device description can be defined from dc measurements if some of the physical parameters are known. The complexity of the circuit required to complete the device description for RF applications depends on the device environment. To investigate the accuracy of the model the simulated and the measured performance of a commercial DGFET have been compared. The simulation and the measurement of a simple mixer circuit were used to assess the large-signal operation of the model. For dc, small-signal, and large-signal modes of operation, the agreement between measured and simulated values is encouraging. The model is currently being applied to other commercial DGFET's and the large-signal algorithm is being extended to permit the analysis of intermodulation distortion.

## Acknowledgment

The authors are grateful to the Plessey Three-Five Group for supplying details of the P35-1310 device.

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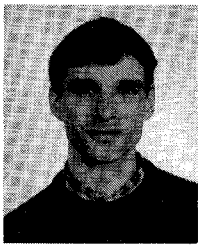

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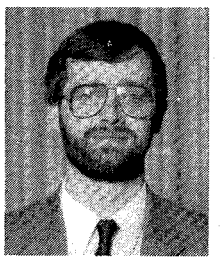
In 1967 he was appointed Lecturer in Electronic Engineering at Leeds and promoted to a senior lectureship in 1976. He has had a great deal of industrial experience both in the United States and the U.K., where from 1980 to 1982 he was the Technical Director of MM Microwave, Kirkbymoorside, Yorkshire, England. He became Head of the Department of Electrical and Electronic Engineering at Leeds University in 1984 and Professor of Electronic Engineering in 1988. In 1969 he set up a Microwave Solid-State Research Group anticipating the importance of high-speed and high-frequency integrated circuits in future radar and communication systems. The group now has 40 active research workers, most of whom are working on collaborative projects with industrial establishments throughout the world. His personal research interests are concerned with the design of microwave devices and subsystems, with a particular interest in the computer-aided design of monolithic integrated circuits. He has also been actively involved in professional further education and is closely involved in the Leeds Microwave Summer School, which attracts 100 industrialists every year for intensive updating in modern electronic system design.

Dr. Howes has published over 100 scientific papers and 16 books, and is currently the European Editor of *Microwave Systems News*. He has lectured widely all over the world and in 1980 was Visiting Professor at Cornell University, Ithaca, NY. He is a fellow of the IEE and a member of the Institute of Physics.



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